

**The paragraph beginning on Page 19, line 22 as follows:**

(Amended) Fig. 65 [64] is a diagram of waveforms showing the operation of the reference voltage generating circuit of Fig. 64.

**The paragraph beginning on Page 46, line 17 as follows:**

In the active state, only during the sense amplifier operation in which large current is consumed, n channel transistor Tr<sub>2</sub> is rendered conductive, resistance of the sensing power supply line is lowered, and floating of the dummy GND line 30 is controlled so as to increase the speed of operation of the sensing operation. In the active period, other than the sense amplifier operating period, other than the sense amplifier operating period, differential amplifying circuit 8 is activated so as to compensate for the floating of the dummy GND line 30 caused by charges flowing in from the I/O line resulting from operation of the column circuitry and to maintain stable potential Vss'. By this combination, it becomes possible to realize lower power consumption and generation of stable potential Vss' higher than the low level of the word lines at the dummy GND line 30.

**The paragraph beginning on Page 48, lines 3 and 21 as follows:**

Fig. 24 is a time charge showing the operation of Fig. 23. As already described with reference to Fig. 102 [57] of the prior art, when the word line WL rises to the boosted voltage Vpp as shown in (a) of Fig. 24, an initial signal is read to the bit line pair BL, BL as shown in (e) of Fig. 24. By sense amplifier activating signals S0 and S0 shown in (b) and (c) of Fig. 24, sense amplifiers 2 and 4 start sensing operation. At this time, comparing circuit 8 is activated by

activating signal S0, compares the level of sense drive line SN with the reference voltage, and cause the dummy GND level generating circuit 19 to discharge until the level of sense drive line SN attains equal to the reference voltage. When the level of the sense drive line SN becomes equal to the reference voltage, discharging operation of dummy GND level generating circuit 19 stops, and potential drop of sense drive line SN stops. Consequently, the potential of sense drive line SN attains to the dummy GND potential  $V_{ss'}$  which is higher than the low level of the word lines, and the potential of the "L" level of bit line  $BL[N]$  attains to the dummy GND potential  $V_{ss'}$ .

**The paragraph beginning on Page 48 and continuing onto Page 49 as follows:**

Fig. 25 shows a second embodiment in accordance with the sixth aspect of the present invention. In this embodiment, the dummy GND level generating circuit 19 generating the dummy GND potential  $V_{[B]ss'}$  is provided separately, and when n channel transistor  $Tr[R]14$  is rendered conductive by sense amplifier activating signal S0, the potential of sense drive line SN is forced to be discharged to the dummy GND potential  $V_{ss'}$ . In the embodiment shown in Fig. 23, it is necessary to provide a comparing circuit 8 and a dummy GND level generating circuit 19 [9] for each sense amplifier. However, in this embodiment shown in Fig. 25, only one dummy GND level generating circuit 19 is necessary for a number of sense amplifiers and what is necessary is to provide an n channel transistor  $Tr14$  for each sense amplifier. Therefore, the arrangement space can be reduced.

**The paragraph beginning on Page 62, line 13 as follows:**

Fig. 38 shows an example in which the embodiment in accordance with a sixth aspect is applied to each memory block. In the example shown in Fig. 38, a plurality of dummy GND lines 51 [41] are provided on a memory block including a number of memory cells (not shown), and a dummy GND level generating circuit 19 is provided outside the memory block 50. The dummy GND potential  $V_{ss'}$  is supplied from dummy GND generating circuit 19 to each dummy GND line 51. Discharging transistors Tr16 are arranged corresponding to dummy GND lines 51, respectively, and the activating signal S0 is applied to the gate of each of the transistors. When the activating signal S0 attains to the "H" level, the dummy GND potential  $V_{ss'}$  generated from the dummy GND generating circuit 19 is supplied to sense drive line SN.